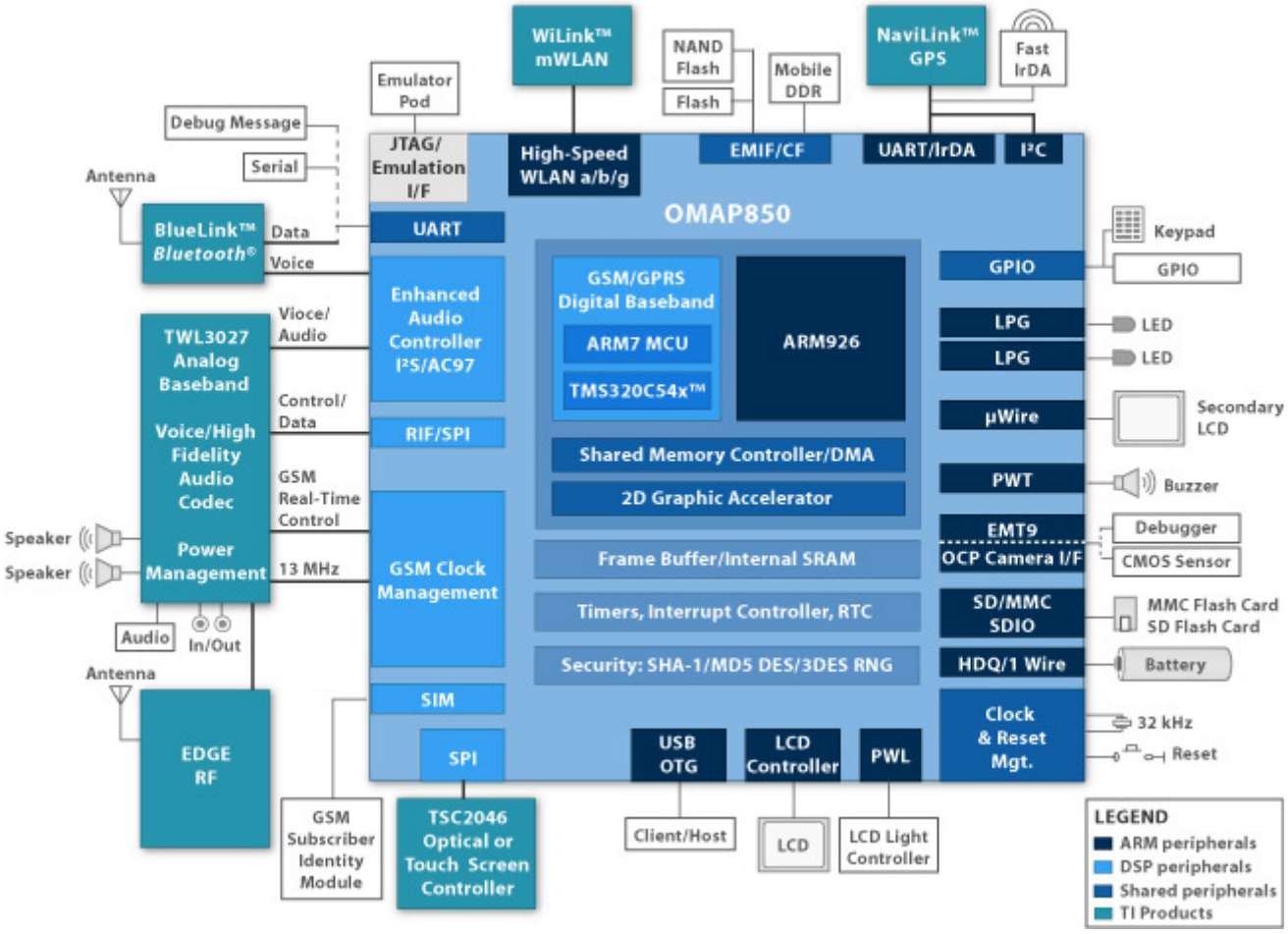
Modem & Applications : OMAP850



Digital Baseband - Availability Disclaimer

The OMAP850 is a single chip that integrates a ARM926EJ-S™ core for applications processing and TI's EDGE digital baseband modem. It is intended for high-volume wireless OEMs and ODMs and is not available through distributors.

The OMAP850 includes all of the features of the OMAP850 and adds support for 128Mb or 256Mb of stacked mobile SDRAM. This makes the OMAP850 well-suited for space-constrained systems or for even smaller, lighter mobile device designs. It also consumes less power than traditional external memory configurations.

With this kind of flexibility, mobile device manufacturers can further reduce the size of high-end, next generation smartphone and wireless handsets. In addition to its space-saving features, stacked SDRAM offers the additional benefit of reduced power consumption - always an important consideration for mobile device designers.

The OMAP850 processor is an integral part of the TCS3500 EDGE chipset solution.

OMAP850 Features:

Low-Power, High-Performance CMOS Technology

- Low-voltage 130 nm technology

- 1.1 - 1.5V cores, 1.8 - 2.75V IO
- Extremely low power consumption: less than 10 µA in standby mode
- Split power supplies for application processing, digital baseband and real-time clock enable precise control over power consumption
- Optimized clocking and power management: Only two clocks required at 13 MHz and 32 kHz

ARM926TEJ Core Subsystem

- ARM926EJ-S V5 architecture up to 200 MHz (maximum frequency)
- 16 kB I-cache; 8 kB D-cache
- Java acceleration in hardware
- Multimedia instruction set architecture (ISA) extension

EDGE Digital Baseband Subsystem

- 384 K-bytes internal SRAM
- E-OTD and TTY support
- Quad vocoder with EFR, FR, HR, AMR
- GSM ultra-low power device (ULPD)
- SIM interface

Application Subsystem

- Supports all leading operating systems
- DMA with 4 physical and 17 logical channels and a dedicated 2D graphics engine
- Programmable GPIO keyboard interface
- 54-Mbps WLAN interface
- Security acceleration in hardware:
    - Secure bootloader
    - 48 kB of secure ROM
    - 16 kB of secure RAM
    - Hardware acceleration for security standards and random number generator
    - Unique die ID cell
    - Third-party Security software library
- Enhanced audio controller (EAC)
- Comprehensive memory controller for interfaces to:
    - 128 MB of mobile SDRAM
    - 256 MB Flash
    - NAND Flash controllers
    - 1.6 Mb ISRAM
- SD/MMC/SDIO interface
- Enhanced Trace Module for debug
- LCD controller
- uWire
- SPI
- 1-wire and HDQ interface
- Bluetooth data/audio interface
- USB On-the-Go
- Two high-speed 3.68 MHz UARTs
- Fast IrDA (FIR)
- Two 32-bit timers
- Parallel camera port
- Programmable three-color LED pulse generation
- I²C master/slave controller
- SmartCard interface

289-ball, 12 mm x 12 mm MicroStar BGA™ Package

Availability Disclaimer

This product is intended for high-volume wireless OEMs and ODMs and is not available through distributors. If your company meets this description, please contact your TI sales office.

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